REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

"The silicon nitride layer 112" as described in the Specification page 10 is recited as the --fourth inter-insulation layer-- in the claims. Accordingly, the Specification has been amended to clarify this.

Further, the "fourth inter-insulation layer" described in the Specification page 11, lines 9-11 have been amended to the --fifth inter-insulation layer-- to avoid ambiguity with the silicon nitride layer 112 or the fourth inter-insulation layer as claimed.

FIG. 4 has been amended to include the reference numeral --112a--, which is described in the Specification page 10, lines 10-16 but inadvertently omitted in the drawings. Replacement of the original sheet of FIG. 4 with the new sheet attached hereto is respectfully requested.

Claims 1-7 are pending in the present application before this amendment. By the present amendment, Claims 1 and 3-6 has have been amended, and Claim 8 has been added. No new matter has been added.

In response to the objection to Claim 4 for containing a term having an improper antecedent basis, the "fourth inter-insulation layer" has been amended to --the **third** inter-insulation layer--. The support for this amendment is found in the Specification page 9, line 21 to page 10, line 2. Withdrawal of the objection is

respectfully requested.

Further, Claim 5 has been amended to depend solely from Claim 1. Thus, the amended Claim 5 no longer follows the multiple dependent claim format. This amendment has been made since a multiple-dependent Claim 5 (without the present amendment) cannot depend from another multiple dependent claim such as Claim 4. Claim 8 (reciting the identical limitations to Claim 5) has been added to depend from Claim 4. No new matter has been added.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by the prior art of FIGS. 1A-1D and the Specification pages 1-4.

In the Specification page 10, lines 12-20, and page 11, lines 15-24, the claimed bit line contacts are formed by a "self-aligned contact mode" which ensures that each "bit line contact" is "formed **only** on the **inside** of **each bit line** defined in a Damascene process, but no on the outside of each bit line" during the bit line contact forming process.

An example of this "self-aligned contact mode" is well shown in FIGS. 2E and 2F. Along the X to X direction in FIG. 2, a bit line is to be formed. The bit line has a width (as shown in FIG. 2F), and the bit line contact 114 is formed substantially entirely on within the area of the bit line 114.

As shown in FIG. 2D and described in the Specification page 10, lines 5-20, a mask pattern (such as the silicon nitride layer 112) is formed on the third inter-insulating layer in such a way that the mask pattern allows the second and third

inter-insulating layers to be etched along the longitudinal length of the bit line and entirely within the width of the bit line. The mask pattern prevents the second and third inter-insulating layers from being etched outside the width of the bit line. This is well illustrated at least in FIG. 2F where the two rounded edges of each bit line contact 114 are extended along the longitudinal length of the bit line, but no such extension is possible outside the width of the bit line.

This is quite substantially different from any prior art, which utilizes photo-resistive patterns over an insulating layer to form a bit line contact as shown in FIG. 1C. There are numerous associated problems with this prior art method, which are well described in the Specification pages 3-4. These problems are solved by the "self-aligned contact mode" utilized in the present application when forming bit line contacts.

Accordingly, Claim 1 has been amended to further clarify the "self-aligned contact mode" of forming bit line contacts.

A step of --**forming a fourth mask pattern by a Damascene process on the third inter-insulation layer, wherein the mask pattern defines etching areas at least substantially along the width of each to-be-formed bit line**-- has been added to Claim 1. The support for this limitation is found at least in the Specification pages 10-11 and FIGS. 2D-2E, 3D-3E, and 4D-4E. For example, in an embodiment described in the Specification and drawings, a silicon nitride layer 112 may be patterned to form the claimed --fourth mask pattern-- (i.e., "the silicon nitride layer

pattern 112a using the photosensitive layer pattern 113 as a mask" see Specification page 10, lines 8-11 and FIG. 4D). This fourth mask pattern (e.g., the silicon nitride patter 112a) would then define the etching areas at least substantially along the width of each to be formed bit line in later step(s). In this regard, this claimed fourth mask pattern provides the "self-aligned contact mode" as it prevents a bit line contact from being formed on the outside of each bit line (see Specification page 10, lines 16-20 and FIGS. 2E-2F). This claimed fourth mask pattern is **not** just a photoresitive layer pattern but is from by a Damascene process, and this quite substantially distinguishes the presently claimed invention from any of the cited prior art teachings.

As the Claim 1 as amended is well supported by the original disclosure of the present application and is considered to be in condition for allowance over the cited prior art teachings, and indication thereof is respectfully requested.

Further, Claim 3 has been amended to further clarify the claimed step of forming the "fourth mask pattern." The support for this amendment is found at least in the Specification page 10, line 5 to page 11, line 20. For example, the claimed fourth inter-insulation layer (such as the silicon nitride layer 112) may be formed on the third inter-insulation layer, which then can be patterned by using a photoresistive layer pattern (such as 113) to form the claimed --fourth mask-- (see FIG. 4D and Specification page 10, lines 5-15).

Claims 1-5 and 7 stand rejected under 35 U.S.C. § 102(e) as being

anticipated by U.S. Patent No. 6,251,726 (Huang). Claims 1-2 and 5-7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,271,125 (Yoo). The "et al." suffix, which may appear after a reference name, is omitted in this paper.

Neither Huang nor Yoo teaches Claim 1, now amended, mainly because none of these cited references teaches, inter alia, the claimed --fourth mask pattern-- that ensures formation of the bit line contacts entirely within the width of the bit line. The Office Action indicates that Huang's metal 42 and Yoo's contact hole opening 29 are allegedly similar to the claimed --bit line contact--; but, regardless, neither Huang (col., 8, lines 5-27; FIG. 7) nor Yoo (as in col. 7, lines 23-38; FIG. 11) discloses, inter alia, the claimed --fourth mask pattern-- formed by a Damacene process (and not just a photorestive layer pattern), which is described in detail above.

For the reasons set forth above, Applicant respectfully submits that Claims 1-8, now pending in this application, are in condition for allowance over the cited references. This amendment is considered to be responsive to all points raised in the Office Action. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of

allowable subject matter. Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

Dated: August 2, 2004

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APPENDIX OF ATTACHMENT

Application Serial No. 10/616,823
Reply to Office Action of May 12, 2004

Replacement Sheet of FIG. 4
(a total of one sheet of drawings)